Application Note XMCGA6T2-AN1/1

Setting Interlaced Resolutions with Windows XP

Publication No. XMCGA6T2-AN1/1 Rev. B

Document History

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NOTE

Refers to NVIDIA GeForce driver version 182.50WHQL.

About This Manual

Conventions

Notices

This manual may use the following types of notice:

CAUTION

Cautions alert you to system danger or loss of data.

NOTE

Notes call attention to important features or instructions.

LINK

Links take you to other documents or websites.

Numbers

All numbers are expressed in decimal, except addresses and memory or register data, which are expressed in hexadecimal. A '0x' prefix indicates a Hexadecimal value. A ‘b’ suffix indicates a Binary value.

Text

Messages from the system are shown in Courier typeface, for instance “`System Description>`”.

Code segments, data structure definitions, function names, parameters etc. are shown in Courier typeface, for instance, `rea_close()`.

Multiple bit fields are numbered from 0 to n where 0 is the least significant, and n the most significant bit.

The terms 'double-word', 'word', 'half-word' and 'byte' mean 64-bit, 32-bit, 16-bit and 8-bit values, respectively.

The terms big-endian and little-endian refer to the way in which multi-byte data is stored in memory. Big-endian data is stored with the most significant byte at the lowest address (68XXX style). Little-endian data is stored with the least significant byte at the lowest address.

The term Pipe refers to a physical aggregation of differential pairs used for a common function that is characterized in terms of the total number of differential pairs. A Pipe is not characterized by the protocol used on it.

Where arrays are referenced, they are written in the form SIGNAL[MSB:LSB] with the most significant bit first.

‘_N’, tilde (~) following the name of a signal denotes that the signal is true or valid when the signal is low.

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LINK
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Abaco will log your query in the Technical Support database and allocate it a unique Case number for use in any future correspondence.

Alternatively, you may also contact Abaco's Technical Support via:

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support@abaco.com

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If you need to return a product, there is a Return Materials Authorization (RMA) form available via the website Support page.

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https://www.abaco.com/support

Do not return products without first contacting the Abaco Repairs facility at the email address below. They will provide specific information needed to complete the RMA form.

LINK
repairs@abaco.com

Contents

1 • Introduction

1.1 Scope

This Application Note describes how to configure the XMCGA6T2 to generate legacy STANAG3350 interlaced resolutions under Microsoft® Windows® XP. The XMCGA6T2 is a double-width XMC/PMC graphics mezzanine module.

This document is concerned with the XMCGA6T2 as supplied as part of an assembly, product nos. X02-ASY-9WC/9YB.

The STANAG3350 standard defines three classes of TV system:

- Class A – 875 line TV system
- Class B – 625 line TV system
- Class C – 525 line TV system

NOTE

Refer to the STANAG3350 standard for further information.

1.2 Related Documents

1.2.1 Abaco

XMCGA6T2-0AB-3 - XMCGA6T2 Interlaced Timings Spreadsheet (provided on request – see Technical Support).

1.2.2 Industry Standard Documents

STANAG3350 - NATO Standardization Agreement (STANAG) Analog Video Standard for Aircraft Systems Applications, Edition 4.

2 • NVIDIA® Driver

NOTE

The XMCGA6T2 has been tested with the NVIDIA GeForce driver version 182.50WHQL. The instructions provided in this application note apply specifically to this version of driver.

CAUTION

Other versions of driver may not operate correctly with the XMCGA6T2.

2.1 Obtaining the NVIDIA Driver

The NVIDIA GeForce driver version 182.50WHQL is available from the NVIDIA website at the following location.

LINK

http://www.nvidia.com/object/winxp_182.50_whql.html

2.2 Installing the NVIDIA Driver

1. Install the NVIDIA driver by double clicking on the .exe file.

NOTE

A restart may be required part way through the installation process if a later version of driver has previously been installed.

2. The NVIDIA driver should then install. Once complete, restart the X02 assembly.

NOTE

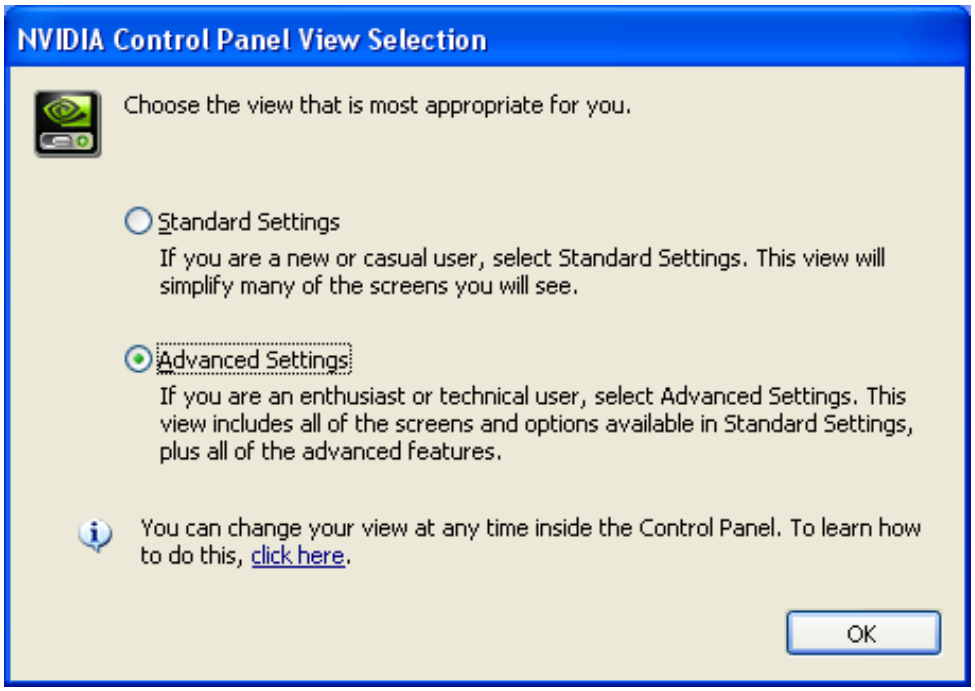
If the setup process asks the question: “The NVIDIA Setup program has detected that one or more Microsoft hardware wizards are active. Do you want to continue with setup?” then Click "Yes" then "Cancel" to terminate the Found New Hardware Wizard.

2.3 Opening the NVIDIA Control Panel

1. Right click on the desktop and select "NVIDIA Control Panel" to open the NVIDIA Control Panel.
2. The following menu will appear the first time the control panel is opened - select "Advanced Settings" and then click "OK".

The NVIDIA Control panel will then appear on the screen:

Figure 2-1 NVIDIA Control Panel



3 • Configuring for Single or Multiple Displays

The XMCGA6T2 FPGA supports two input modes:

- Common MIO Input
- Separate MIO Input

Common MIO Input – in this mode the G73 GPU is configured for a single display which is replicated across all four analog RGB outputs (VGA1-4).

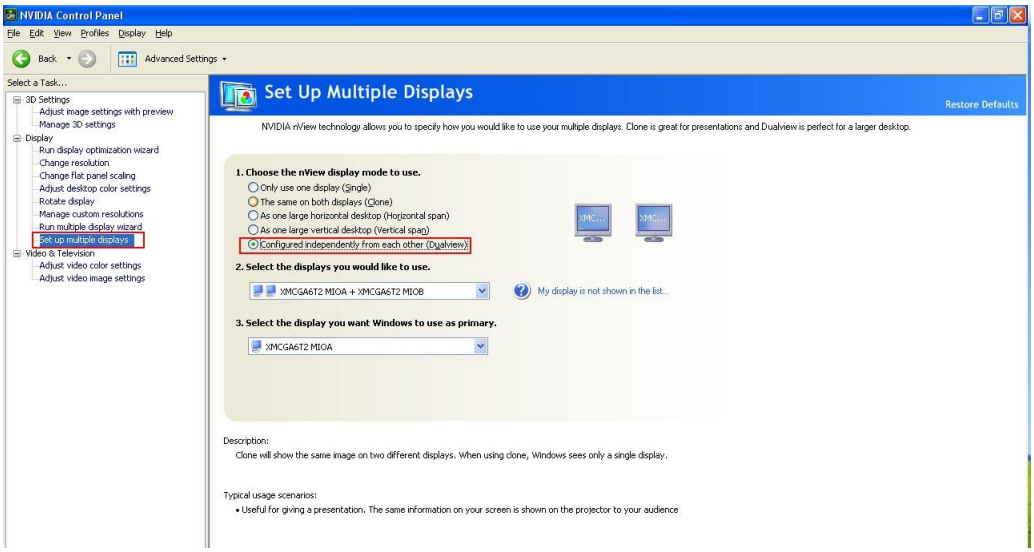
Separate MIO Input – in this mode the G73 GPU is configure for multiple (two) displays with the primary display (MIO A) being replicated across analog RGB outputs (VGA1 & 3) and the secondary display (MIO B) being replicated across analog RGB outputs (VGA2 & 4).

The FPGA input mode is selected using the FT4 backplane strap option, on pin 52 of the P14 connector. The NVIDIA Control Panel will detect either one or two displays depending on the setting of this strap option.

3.1 Multiple Display Configuration

1. Open the NVIDIA Control Panel
2. Select “Set up multiple displays” from the list on the left side of the screen:

Figure 3-1 Setting Up Multiple Displays

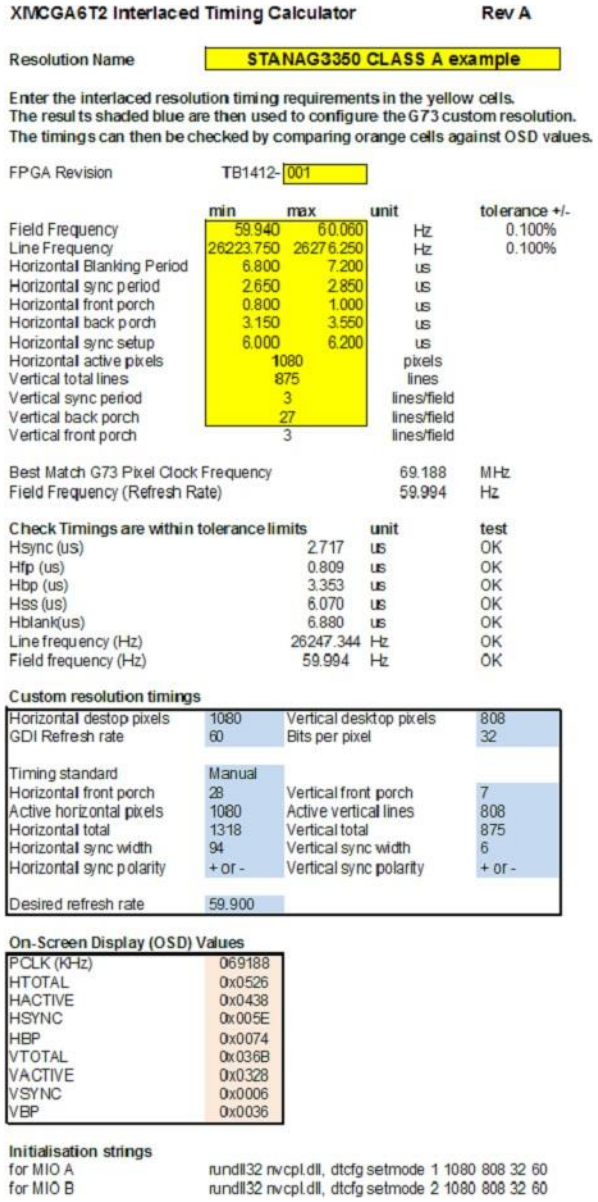


3. Select “Configured independently from each other (Dualview)” as shown in red in the diagram above.
4. Click “Apply” on the bottom right of the screen to commit the changes.
5. Each display should now be capable of being configured independently.

4 • Custom Resolutions

4.1 Calculating STANAG3350 Timings for Custom Resolutions

Figure 4-1 XMCGA6T2-0AB-3 Interlaced Timings Spreadsheet



XMCGA6T2 Interlaced Timing Calculator **Rev A**

Resolution Name	STANAG3350 CLASS A example

Enter the interlaced resolution timing requirements in the yellow cells.
The results shaded blue are then used to configure the G73 custom resolution.
The timings can then be checked by comparing orange cells against OSD values.

FPGA Revision TB1412-001

	min	max	unit	tolerance +/-
Field Frequency	59.940	60.060	Hz	0.100%
Line Frequency	26223.750	26276.250	Hz	0.100%
Horizontal Blanking Period	6.800	7.200	us	
Horizontal sync period	2.650	2.850	us	
Horizontal front porch	0.800	1.000	us	
Horizontal back porch	3.150	3.550	us	
Horizontal sync setup	6.000	6.200	us	
Horizontal active pixels	1080		pixels	
Vertical total lines	875		lines	
Vertical sync period	3		lines/field	
Vertical back porch	27		lines/field	
Vertical front porch	3		lines/field	

Best Match G73 Pixel Clock Frequency	69.188	MHz
Field Frequency (Refresh Rate)	59.994	Hz

Check Timings are within tolerance limits		unit	test
Hsync (us)	2.717	us	OK
Hfp (us)	0.809	us	OK
Hbp (us)	3.353	us	OK
Hss (us)	6.070	us	OK
Hblank(us)	6.880	us	OK
Line frequency (Hz)	26247.344	Hz	OK
Field frequency (Hz)	59.994	Hz	OK

Custom resolution timings

Horizontal destop pixels	1080	Vertical desktop pixels	808
GDI Refresh rate	60	Bits per pixel	32
Timing standard	Manual		
Horizontal front porch	28	Vertical front porch	7
Active horizontal pixels	1080	Active vertical lines	808
Horizontal total	1318	Vertical total	875
Horizontal sync width	94	Vertical sync width	6
Horizontal sync polarity	+ or -	Vertical sync polarity	+ or -
Desired refresh rate	59.900		

On-Screen Display (OSD) Values

PCLK (KHz)	069188
HTOTAL	0x0526
HACTIVE	0x0438
HSYNC	0x005E
HBP	0x0074
VTOTAL	0x036B
VACTIVE	0x0328
VSYNC	0x0006
VBP	0x0036

Initialisation strings

for MIO A	rundll32 nvcpl.dll, dtcfg setmode 1 1080 808 32 60
for MIO B	rundll32 nvcpl.dll, dtcfg setmode 2 1080 808 32 60

The XMCGA6T2-0AB-3 Interlaced Timings Spreadsheet is used to calculate G73 video timings for a particular STANAG3350 resolution. The STANAG3350 timings required by the display are entered in the yellow cells and the spreadsheet then calculates the corresponding G73 timings and displays these in the blue cells.

1. Check that all entries in the “test” column on the spreadsheet are displayed as OK – if any display ERROR, then the required timings cannot be achieved – either relax the timing requirements and/or change the Horizontal active pixels setting and try again.

Examples are provided for typical STANAG3350 Class A, B, & C displays which can be used as the starting point. If you start from the example corresponding to the class of display you need to drive, it should only be necessary to change the number of horizontal active pixels as all other timings are defined by the STANAG3350 standard.

Because the STANAG3350 standard does not define the pixel counts for horizontal timings it is likely that some adjustment of the display and/or G73 timings will be necessary to achieve a correctly sized and centered display.

Many STANAG3350 displays are designed to tailored or modified versions of the STANAG3350 standard – it is advisable to consult the display manufacturer to determine what the video input requirements are for each STANAG3350 display.

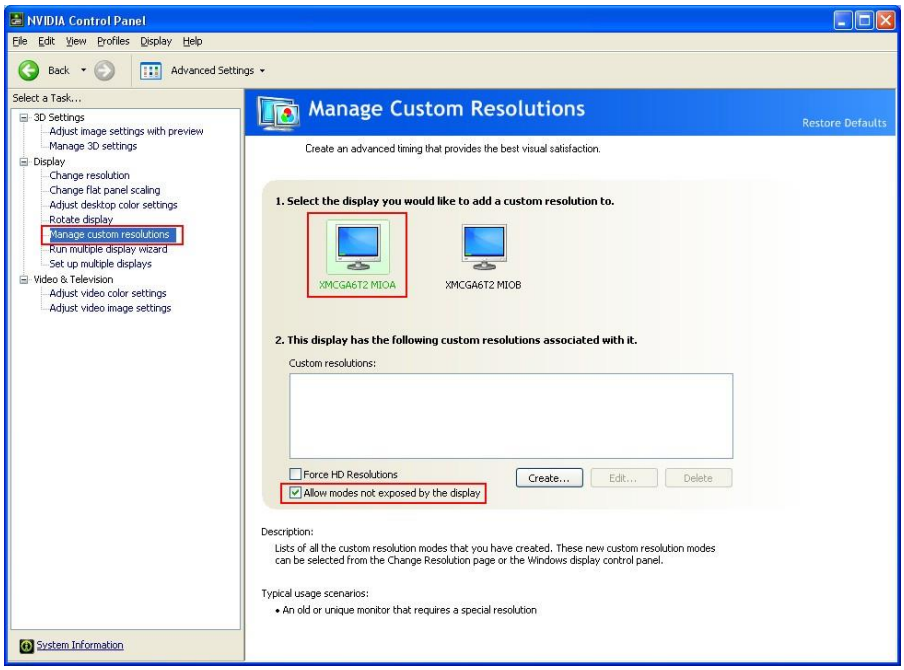
The cells highlighted in orange provide OSD values for debugging (see Chapter 5, "Verifying Timings Using the On-Screen Display (OSD)").

2. Ensure that the FPGA revision entered in the first cell matches that of the target board (see Chapter 5, "Verifying Timings Using the On-Screen Display (OSD)" for details of how to display the FPGA revision using the OSD). Different timing values may be required for early pre-production prototype boards – the spreadsheet uses this value to adjust timings (if necessary).

4.2 Enabling Custom Resolutions

1. Open the NVIDIA Control Panel
2. In the NVIDIA control panel, select "Manage custom resolutions" from the panel on the left-hand side of the screen. The following screen should appear:

Figure 4-2 Enabling Custom Resolutions on MIO A



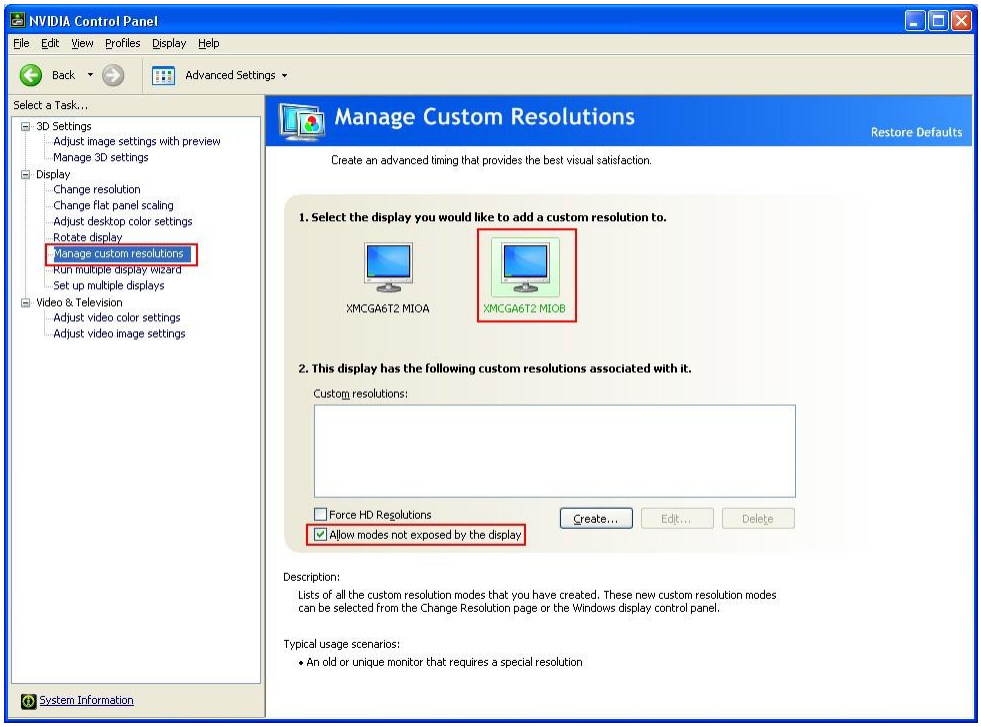
3. Ensure that “XMCGA6T2 MIOA” is selected as the display to make changes to.
4. Tick the box marked “Allow modes not exposed by the display”.
5. Click “Apply” in the bottom right corner to confirm the changes.

NOTE

It is essential that this is carried out before any custom resolution parameters are added.

6. Repeat steps 3-5 above for “XMCGA6T2 MIOB” (if using multiple displays). The screen should be as below:

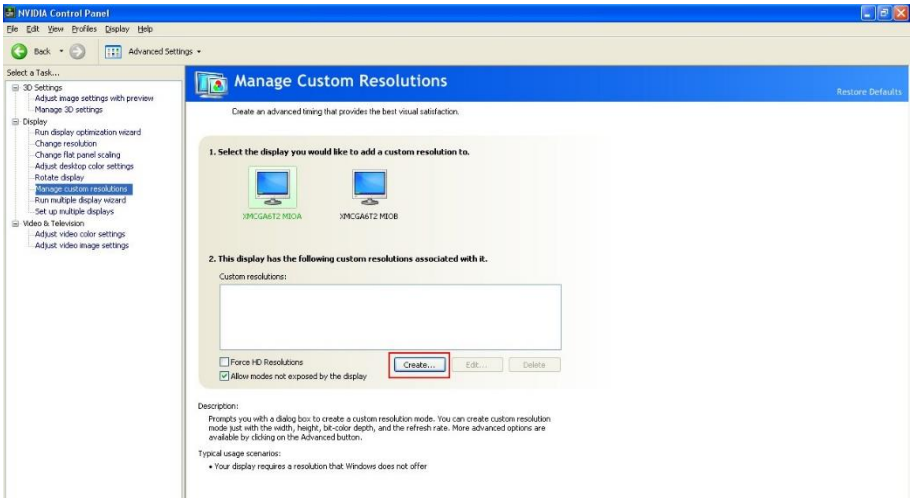
Figure 4-3 Enabling Custom Resolutions on MIO B



4.3 Adding Custom Resolutions

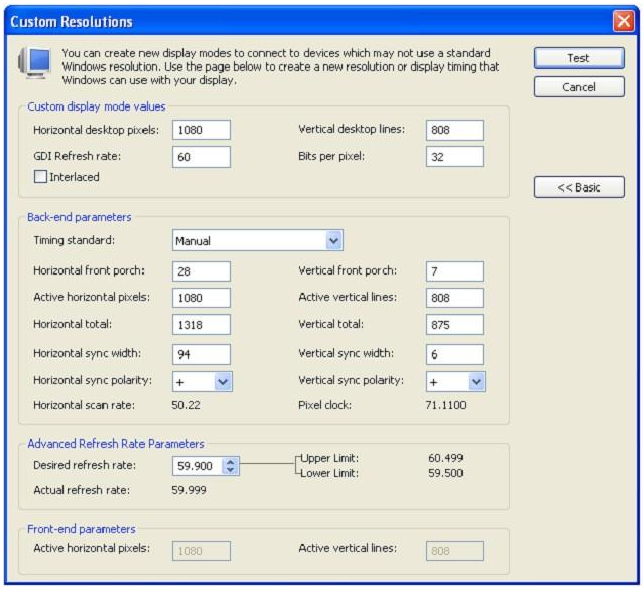
1. Open the NVIDIA Control Panel, select “Manage custom resolutions” and then select which MIO port you want to add the custom resolution to.
2. Click the “Create” button in the center of the screen (see below:)

Figure 4-4 Adding Custom Resolutions



3. Click the “Advanced >>” tab on the right-hand side of the screen and enter the timing parameters from the Timing Calculator Spreadsheet (see Section 4.1, "Calculating STANAG3350 Timings for Custom Resolutions") into the Custom Resolutions form. The figure below shows an example, but substitute the numbers from the spreadsheet:

Figure 4-5 Entering Custom Resolution Parameters (Class A Example)



NOTES

Do not tick the Interlaced box. The horizontal and vertical sync polarities can be set to either + or – as the output sync polarity is controlled by the FPGA.

Displayed parameters such as the Pixel clock, Horizontal scan rate and Actual refresh rate are not accurate – use the OSD to verify exact timings.

4. Select “Test”, the custom resolution will be output on the MIO port.
5. Use the On-Screen Display to verify that the timings are correct (see Chapter 5, “Verifying Timings Using the On-Screen Display (OSD)”. If the display times out press “Test” again. If the pixel clock frequency reported by the OSD doesn’t match that predicted by the spreadsheet it may be necessary to increment/ decrement the “Desired Refresh Rate” setting by 0.100 Hz and repeat by pressing “Test” again.
6. Once the timings are correct, select “Yes”; this will add the custom resolution for that MIO port.

NOTE

The option for editing an existing custom resolution does not operate correctly in this version of NVIDIA driver – current values are not correctly loaded and consequently it is necessary to check all values when using the edit option and re-enter all that are incorrect, not just the ones you want to change.

4.4 Selecting the Custom Resolution for Output

1. Once the custom timings have been added, the Manage Custom Resolutions tabs should be similar to those shown below. In this example separate custom resolutions have been added to both MIOA and MIOB for STANAG3350 A, B & C resolutions:

Figure 4-6 Selecting Custom Resolutions for Output

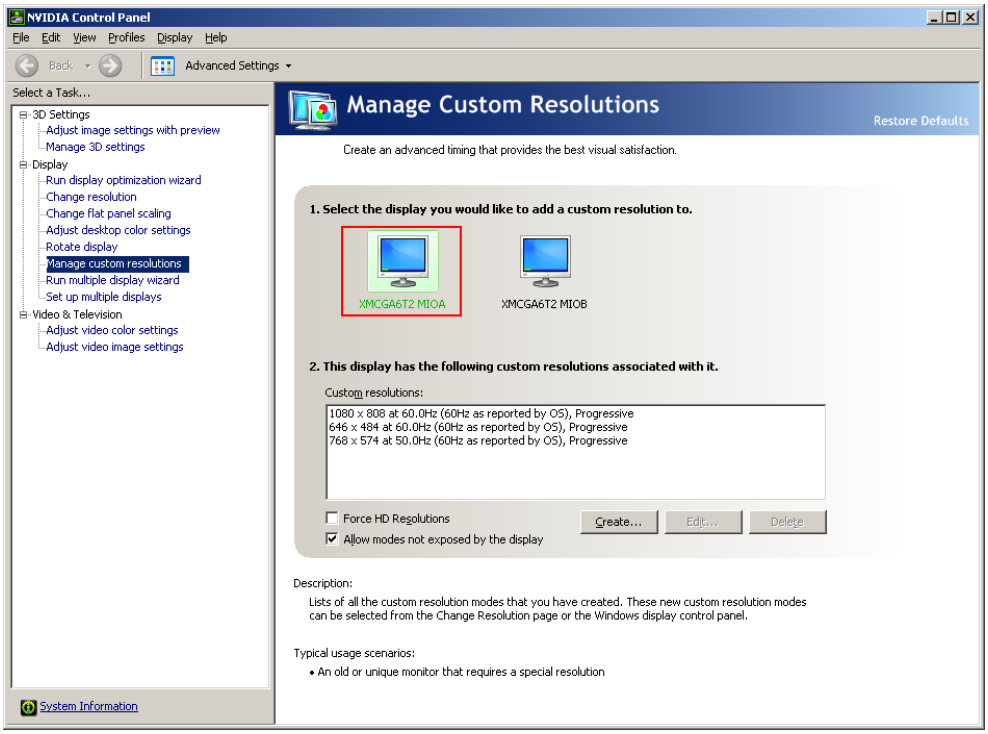
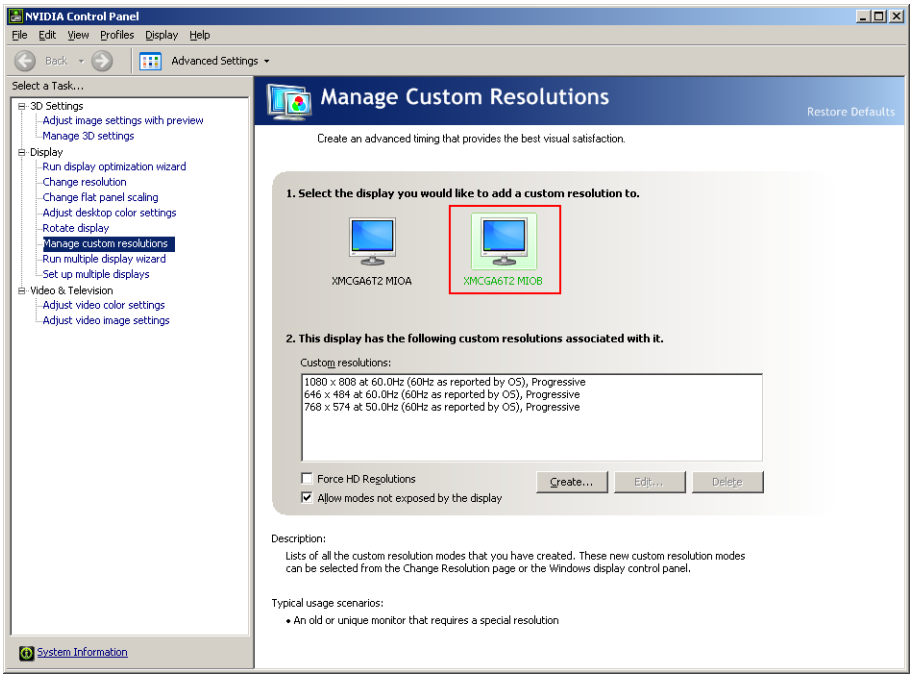
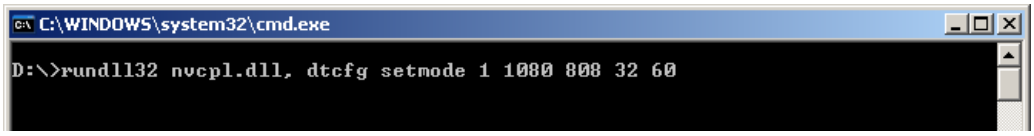


Figure 4-7 Selecting Custom Resolutions for Output



2. Open a command prompt by going to the Start menu and selecting “run”.
3. Type “cmd” in the box, the following window should appear:

Figure 4-8 DOS Command Window



4. A custom resolution can now be selected for MIO A or MIO B by entering the following command in the DOS box:

   `rundll32 nvcpl.dll, dtcfg setmode [a] [b] [c] [d] [e]`

   where:

   a. = display head, 1 = MIOA, 2 = MIOB

   b. = number of horizontal pixels

   c. = number of vertical lines

   d. = number of bits per pixel (bpp)

   e. = refresh rate in Hz

NOTE

Refer to the initialization strings at the bottom of the Timing Calculator spreadsheet for actual values.

An example for STANAG3350 A on MIO port A is:

```
rundll32 nvcpl.dll, dtcfg setmode 1 1080 808 32 60
```

Alternatively, individual batch files may by created with the command lines above to output the corresponding standard on the desired monitor by double clicking the batch file.

5 • Verifying Timings Using the On-Screen Display (OSD)

Figure 5-1 On-Screen Display

The XMCGA6T2 can generate an On-Screen Display overlay in the top left-hand corner of each display. The OSD is generated by the XMCGA6T2 FPGA and it displays the G73 timings that the FPGA is measuring on its respective MIO port. This display can be used to verify that the custom resolution timings have been entered correctly by comparing the displayed values against the cells highlighted in orange on the Interlaced Timings Calculator spreadsheet.

Because the OSD timing values give the timings at the MIO port inputs to the FPGA they do not change if the FPGA force bypass strap is changed.

If a mistake is made in entering STANAG3350 timings a stable display may not be produced on the STANAG3350 monitor – in this situation it is not possible to see the OSD values to figure out what is wrong. In this situation the Force Bypass strap can be applied, and a multi-sync progressive monitor connected in place of the STANAG3350 monitor – this should then display the OSD values and enable the fault to be diagnosed.

The Force Bypass mode is selected using the FT3 backplane strap option, by grounding pin 23 of the P14 connector.

The OSD also displays the revision of FPGA firmware TB1412-xxx, where xxx is the revision (001 in the above figure).

The pixel clock frequency is also displayed in kHz – this may differ by up to +/- 1 (kHz) from the spreadsheet value due to measurement accuracy limitations within the FPGA.

The OSD is enabled using the FT2 backplane strap option (pin 24 of the P14 connector) – when this pin is unconnected the OSD is disabled, and when connected to GND the OSD is enabled.

Abaco Systems Information Centers

Americas:
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Additional Resources

For more information, please visit the Abaco Systems web site at:

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