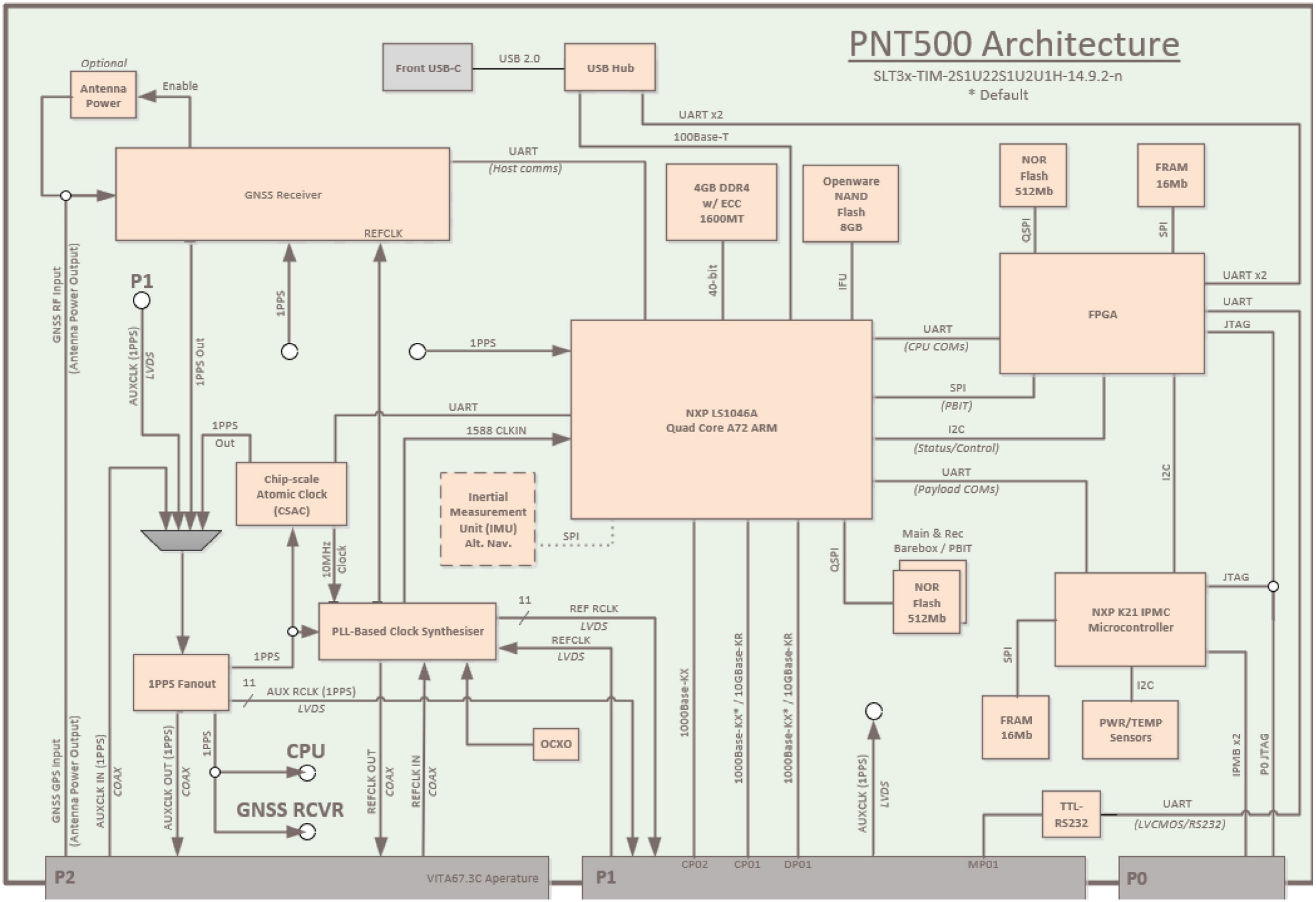
PNT500 Architecture
SLT3x-TIM-2S1U22S1U2U1H-14.9.2-n
* Default
Optional
Antenna Power
Enable
Front USB-C
USB 2.0
USB Hub
UART x2
100Base-T
GNSS Receiver
UART
(Host comms)
REFCLK
4GB DDR4 w/ ECC 1600MT
Openware NAND Flash 8GB
NOR Flash 512Mb
FRAM 16Mb
QSPI
SPI
FPGA
UART x2
UART
JTAG
40-bit
IFU
P1
GNSS RF Input
(Antenna Power Output)
AUXCLK (1PPS)
LVDS
1PPS Out
1PPS
1PPS
NXP LS1046A Quad Core A72 ARM
UART
(CPU COMs)
SPI
(PBIT)
I2C
(Status/Control)
UART
(Payload COMs)
UART
1588 CLKIN
1PPS Out
Chip-scale Atomic Clock (CSAC)
Inertial Measurement Unit (IMU) Alt. Nav.
SPI
10MHz Clock
Main & Rec Barebox / PBIT
NOR Flash 512Mb
QSPI
I2C
JTAG
NXP K21 IPMC Microcontroller
PLL-Based Clock Synthesiser
11
REF RCLK
LVDS
REFCLK
LVDS
1PPS Fanout
1PPS
11
AUX RCLK (1PPS)
LVDS
SPI
I2C
FRAM 16Mb
PWR/TEMP Sensors
OCXO
CPU
GNSS RCVR
GNSS GPS Input
(Antenna Power Output)
AUXCLK IN (1PPS)
COAX
AUXCLK OUT (1PPS)
COAX
1PPS
REFCLK OUT
COAX
REFCLK IN
COAX
1000Base-KX
1000Base-KX* / 10GBase-KR
1000Base-KX* / 10GBase-KR
AUXCLK (1PPS)
LVDS
TTL-RS232
UART
(LVCMOS/RS232)
IPMB x2
P0 JTAG
P2
VITA67.3C Aperature
P1
CP02
CP01
DP01
MP01
P0